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10/749,766	12/30/2003	Sang-Hoon Hong	51876P557	9102

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 08/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,766	HONG ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4 and 6-8* is/are rejected.

7)☒ Claim(s) *3 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 1-8 are pending in the Application.

Claims 1-8 have been amended.

Claims 1-2, 4, and 6-8 are rejected.

Claims 3 and 5 are objected to.

Response to Amendment

2. Applicant's amendments and arguments filed on 26 May 2006 in response to the office action mailed on 23 February 2006 have been fully considered, but they are not persuasive. Therefore, the rejections made in the previous office action are maintained, and restated below, with changes as needed to address the amendments.

Claim Objections

3. Claims 3-6 are objected to because of the following informalities

As for claim 3, the phrase "number of unit tag," as recited on the line 6 of this claim should be replaced with the phrase "number of unit tag blocks," for clarity.

As for claim 6, Examiner recommends Applicant add the word "indicating" or "designating" between the word "information" and "which" in line 3 of this claim for clarity.

Claims 4 and 5 are objected to for further limiting claim 3.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 4, 6, 7, and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 recites the limitation "the information" in line 13 of page 3. There is insufficient antecedent basis for this limitation in the claim. More specifically, claim 3 recites "address information" on line 1 of page 3, and claim 1 recites "information" in line 15 of page 2. Which of the two is "the information " as per claim 4 referring to?

Claim 7 recites the limitation "the information" in lines 8-9 of page 4. There is insufficient antecedent basis for this limitation in the claim. More specifically, "an information" is set forth in line 6 of for *each* logical block address. Which of the information corresponding to each of the M number of logical block addresses is being referred to here?

Claim 6 is rejected for further limiting claim 4, hence inheriting the deficiencies of the claim.

As for claim 8, the phrase "wherein the refresh operation is performed except for the address representing the M number of the predetermined word lines" as recited in the final two lines of page 4 renders the claim indefinite, as one of ordinary skill in the

art would be unable to ascertain the metes and bounds of this claim limitation. More specifically, it is unclear how a refresh operation can be performed "except for [an] address ...". Examiner however assumes Applicant intended to describe performing the refresh operation on all word lines except for those corresponding to the address representing the M number of the predetermined word lines.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 2 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Burger et al. (US Patent 6,557,080 B1), hereinafter Burger.

As for claim 1, Burger teaches a semiconductor device for refreshing data stored in a memory device, comprising:

a cell area (Fig. 1, element 16) having N+1 number (in this example, 6) of unit cell blocks (element 20), each including M number of word lines which respectively are coupled to a plurality of unit cells (elements 24) – col. 4, lines 34-47. Note since the specification defines M as any positive integer, the number of word lines can be *any* positive integer. Though the word lines are not illustrated

in Fig. 1, word lines are inherently part of a cache memory – wherein the N number of unit cell blocks are corresponded to logical cell block addresses and one unit cell block is added for accessing data with high speed (col. 4, lines 48-67 – the tag memory is used to map addresses (i.e. logical to physical and physical to logical addressing mapping. Also note since the plurality of unit cells comprise a cache, all unit cell blocks (including the $(N+1)^{th}$ block (i.e. one unit cell block added per this claim) is used for accessing data with high speed));

a tag block having N+1 (in this example, 6) number of unit tag blocks, each unit tag block storing at least one physical cell block address storing data ((Fig. 1, element 28) – col. 4, lines 48-62 – each tag block stores address information on each unit cell block (i.e. row of the cache memory) in order to execute address mapping), wherein the tag block receives a logical cell block address designated for accessing one of N number of unit cell blocks and converts the logical cell block address into a physical cell block address designated for accessing one of the N+1 number of unit cell blocks (referring again to col. 4, lines 48-67, the processor accessing data stored in the unit cell blocks by first accessing the corresponding tag block (Fig. 1, element 28), the tag block is used to receive the logical address in order to properly map it to its corresponding physical address. Once the physical address is determined the processor can properly access the unit cell block); and

a control means (Fig. 1, element 18) for controlling the tag block and the predetermined cell block table (the cache control circuitry is used to control the

subblock table (element 30) and the tag block (element 28)) and the for refreshing the data in the plurality of unit cells coupled to a word line in response to the at least one physical cell block address (col. 3, line 66 through col. 4, line 5 – the control circuitry is used to refresh the cache) – The control circuitry uses the tag blocks and table to address the block or subblocks that require refreshing.

wherein the tag block stores information representing the converted physical cell block address and a refresh operation is preformed through the use of the information (information stored in each unit tag block is used to locate the corresponding data via addressing mapping (i.e. logical to physical) – col. 4, lines 53-67. Also note the information (i.e. address mapping information) must be used by the processor for the refresh operation of the cells, otherwise the processor would be unable to refresh the memory (col. 3, line 66 through col. 4, line 5)).

As for claim 2, Burger teaches the semiconductor device as recited in claim 1, further comprising:

a predetermined cell block table (Fig. 1, element 30) for storing information representing at least more than one word line among the M number of the word lines storing data (the subblock table stores information for each subblock – col. 4, line 63 through col. 5, line 6). In other words, the table stores information, which includes as a whole, more than one word line among the M word lines, as each unit cell block contains one or more word lines. Even if any

given unit cell block contains only one word line, the table still stores more than one word line as each of the plurality of unit blocks must contain at least one word line.

As for claim 7, Burger teaches a method for a refresh operation of a semiconductor memory device including a cell area (Fig. 1, element 16) having N+1 number (in this example, 6) of unit cell blocks (element 20), each including M number of word lines which respectively are coupled to a plurality of unit cells (elements 24) – col. 4, lines 34-47. Note since the specification defines M as any positive integer, the number of word lines can be any positive integer. Though the word lines are not illustrated in Fig. 1, word lines are inherently part of the cache memory; a tag block having N+1 (in this example, 6) number of unit tag blocks, each having M number of registers for sensing an update of data (col. 4, line 53 through col. 5, line 6) – each unit tag block holds information on each unit block (element 20) in a one-one correspondence. This information is used, among other things, to determine if data desired by the processor is still valid (i.e. requiring update/refresh or not), comprising the step of:

(A) starting a refresh mode in response to a refresh signal (refresh mode begins when the processor requests data. The data may then be refreshed if needed- col. 3, line 66 through col. 4, line 5 and col. 4, lines 63-67). Note in the cited lines, Burger discusses refreshing the cache via requests from the processor according to techniques known in the art. It is well known in the art that some type of refresh signal must be applied in order to instantiate the refresh

of the memory (i.e. the processor cannot possibly require a refresh of the memory without a some sort of signal instructing the memory to do so – i.e. the cache is not auto-refreshing);

(B) finding at least one physical cell block address and word line determined by the physical cell block address having data by checking (N+1) X M number of registers in the tag block, each register storing logical block address and an information representing an update of the logical block address (Fig. 2, element 30 depicts the subblock use table. The table stores information on each subblock contained in the cache col. 4, line 53 through col. 5, line 6 (each subblock has its own bit)). In other words the table contains a number of registers equal to the number of rows (i.e. N+1) times columns in the cache. The table is used to verify which data is valid (i.e. which will require updating or refreshing). Again there is a one-one correspondence for each entry in the table and the subblock within the cache, therefore the table is not only used to store the validity of the data, but can also be used to locate exactly which subblock to which its referring. The tag block is used to store the updated logical to physical address mapping information); and

(C) performing the refresh operation in through the use of the information (refresh is performed on the cache - col. 3, line 66 through col. 4, line 5). Again the cell, which is to be refreshed, must be selected (via the table) before the refresh operation can be performed. The mapping information is the information needed in order to identify the correct memory location to refresh.

wherein the N number of unit cell blocks are corresponded to addresses and one unit cell block is added for accessing data with high speed (col. 4, lines 48-67 – the tag memory is used to map addresses (i.e. logical to physical and physical to logical addressing mapping). Also note since the plurality of unit cells comprise a cache, all unit cell blocks (including the Nth + 1 block (i.e. one unit cell block added per this claim) is used for accessing data with high speed)).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burger (US Patent 6,557,080 B1) as applied to claim 7 above, and in further view of Benedix et al. (US PG Publication 2002/0141272 A1), hereinafter Benedix.

Though Burger teaches all the limitations of claim 7, he fails to disclose denoting M number of registers in a predetermined cell block table in order to find out an address representing M number of predetermined word lines among (N+1)*M word lines of the N+1 number of unit cell blocks, wherein the refresh operation is performed except for the address representing the M number of the predetermined word lines.

Benedix however teaches a dynamic semiconductor memory with refresh and method for operating such a memory. In his disclosure, Benedix teaches in paragraph 0018 (all lines) memory cells disposed in rows and word lines. Further, the control device can selectively refresh word lines by resetting all of the word lines and only refreshing the selected ones. Further detail of the refresh operation is provided in paragraph 0020, lines 1-13.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Burger to further include Benedix's memory with refresh into his own cache with dynamic control sub-block fetching. By doing so, Burger would benefit by improving the refresh operation of his memory cells, hence improving the overall memory access readiness of the memory as taught by Benedix in paragraph 007 (lines 1-9).

Response to Arguments

7. Applicant's arguments with respect to claim 1, 2, 7, and 8 have been considered but are not found to be persuasive.

As for claims 1, 2, and 7, Applicant alleges that Burger does not disclose, teach or suggest a cell area having N+1 number of unit cell blocks, each including M number of words lines which respectively are coupled to a plurality of unit cells wherein the N number of unit cell blocks are corresponded to address and one unit cell block is added for accessing data with high speed. Applicant however provides not further specific arguments and/or contrasting evidence with

respect to Burger's teachings other than a general assertion that such a limitation is not present.

Examiner however maintains, per the rejection *supra*, that Burger in fact does teach the following limitations:

> a cell area (Fig. 1, element 16) having N+1 number (in this example, 6) of unit cell blocks (element 20), each including M number of word lines which respectively are coupled to a plurality of unit cells (elements 24) – col. 4, lines 34-47. Note since the specification defines M as any positive integer, the number of word lines can be *any* positive integer. Though the word lines are not illustrated in Fig. 1, word lines are inherently part of a cache memory – wherein the N number of unit cell blocks are corresponded to logical cell block addresses and one unit cell block is added for accessing data with high speed (col. 4, lines 48-67 – the tag memory is used to map addresses (i.e. logical to physical and physical to logical addressing mapping.

Applicant additionally contends that Burger fails to teach, "the N number of unit cell blocks are corresponded to addresses and one unit cell block is addressed for accessing data with high speed". Examiner however maintains that Burger does in fact teach unit cell blocks for accessing data with high speed. More specifically, all unit cell block of the disclosure are used within a cache. A cache (as is well known in the art) is a memory device used for high speed access of data. Examiner further contends that not only is the $(N+1)^{th}$ block used

for accessing data with high speed, but the remaining N blocks are in fact also used for high speed data access since they are among the constituent parts of Burger's cache.

As for claim 8, Applicant asserts that the combined teachings of Burger and Benedix fail to disclose all limitations of the claim. More specifically, it is Applicant's contention that Benedix fails to cure the alleged deficiencies of Burger's teachings with respect to claim 7. This argument however is not found to be persuasive as Examiner maintains that Burger in fact anticipates claim 7 per the rejection and arguments discussed *supra*.

Conclusion

8. Claims 3 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

10. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Craig E Walter
Examiner
Art Unit 2188

CEW

Reginald G. Bragdon
REGINALD BRAGDON
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100